Development of a Pipeline CAMAC controller with PC104plus single board computer

Project team

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Architecture of Pipeline CAMAC Controller

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Pipeline CAMAC Controller

CAMAC reply frames

Pipeline CAMAC Controller

TX

RX
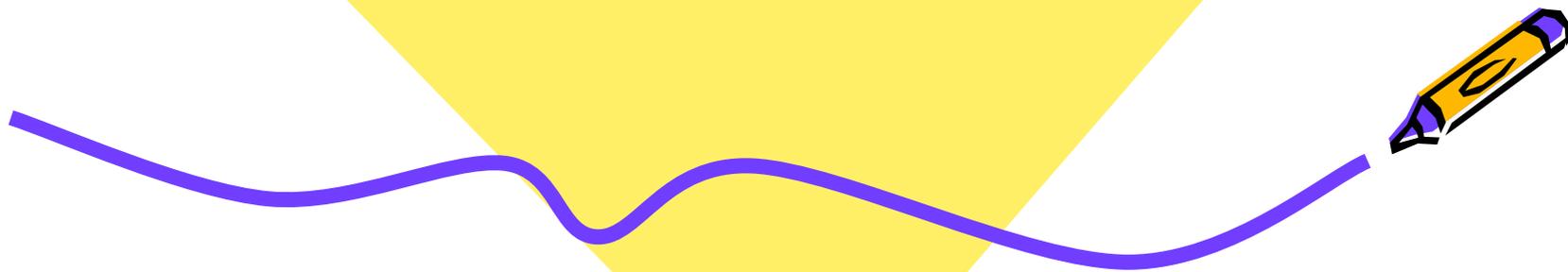
CAMAC command frames

The controller gets a command frame from RX via CAMAC command FIFO,
executes the frame in a 1 usec. and
puts a reply frame to TX via CAMAC reply FIFO.
The command frame and the reply frame contain CAMAC N, A, F,
Status (Q,X) and 24-bit data.

Pipeline Object Controller

Pipeline Object Controller

RX

TX

Point to Point link

| Object command |
| Object reply |

N x M network

| DST | SRC | Object command |
| DST | SRC | Object reply |
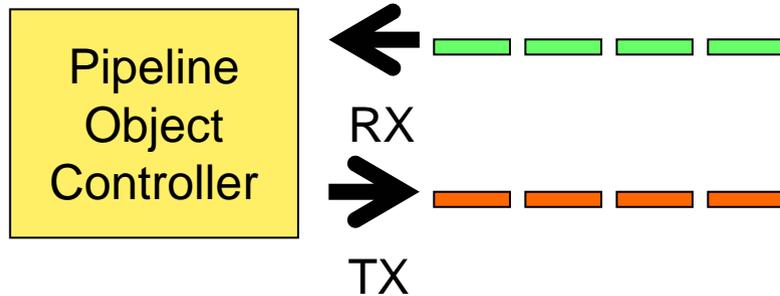
Examples of configuration

CAMAC ↔ PC

FADC ↔ NETWORK ↔ PC
FADC ↔ NETWORK ↔ PC
FADC ↔ NETWORK
CAMAC ↔ NETWORK ↔ FPGA
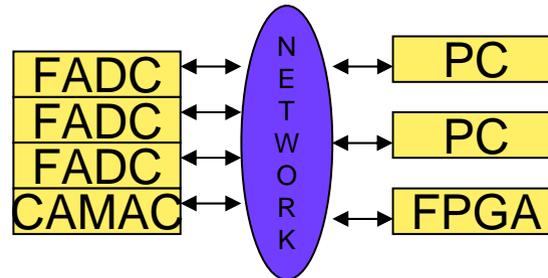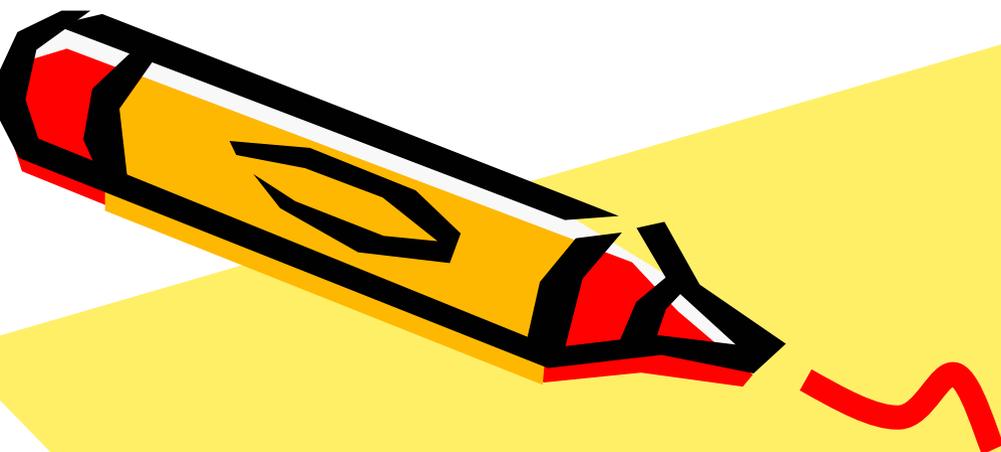
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# Overview of the CAMAC controller
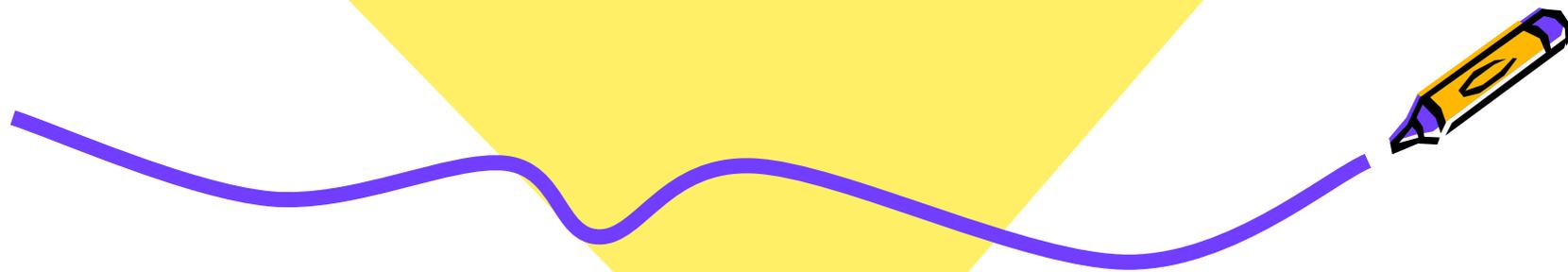
Pipeline CAMAC Controller
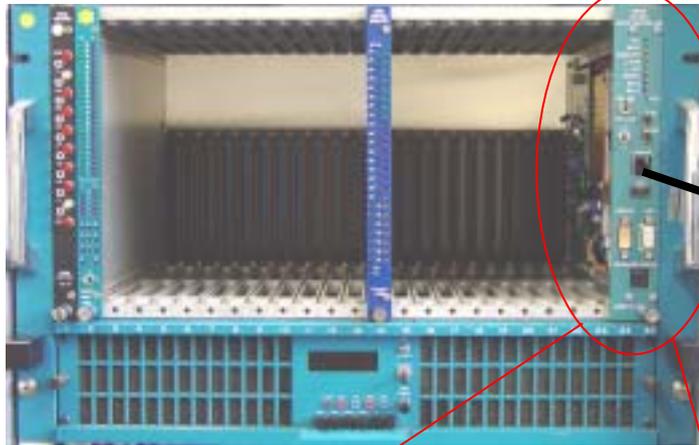
Fast Ethernet

**PC104plus PC board computer
PCM-9370's Crusoe TM5400,
Memory, Flash Disk, Ethernet,
USB, …**

**ALTERA FPGA for PCI
ALTERA FPGA for CAMAC**

CAMAC/DAQ functions

- Basic CAMAC operation
- LAM interrupt function
- Trigger Input and Busy Out with Event counter
- Trigger Interrupt function

PCI registers for CAMAC

Registers
2 32-bit TX/RX data registers
TX/RX Control and Status registers
TX/RX Memory Address registers
TX/RX Preset Transfer counters
TX/RX Actual Transfer counters
TX/RX FIFO count registers

Operation modes
Programmed I/O
Block transfer

PCI logic

PCI logic

CAMAC/DAQ logic

Altera FPGA

CAMAC executor

CAMAC Interrupt

DAQ executor

DAQ Interrupt

Packet control

CMD FIFO

REPLY FIFO

PCI logic

CAMAC

DAQ

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CAMAC/DAQ Frame format

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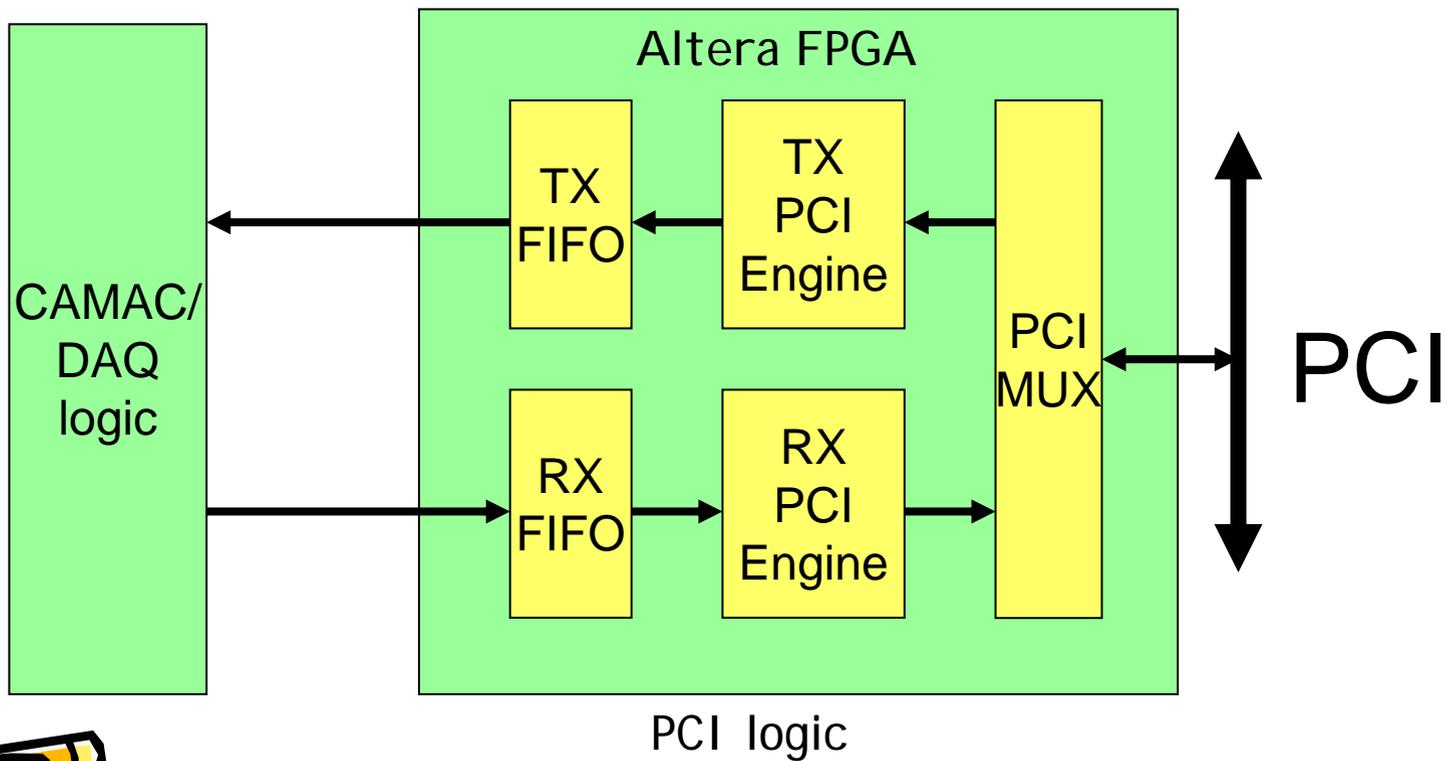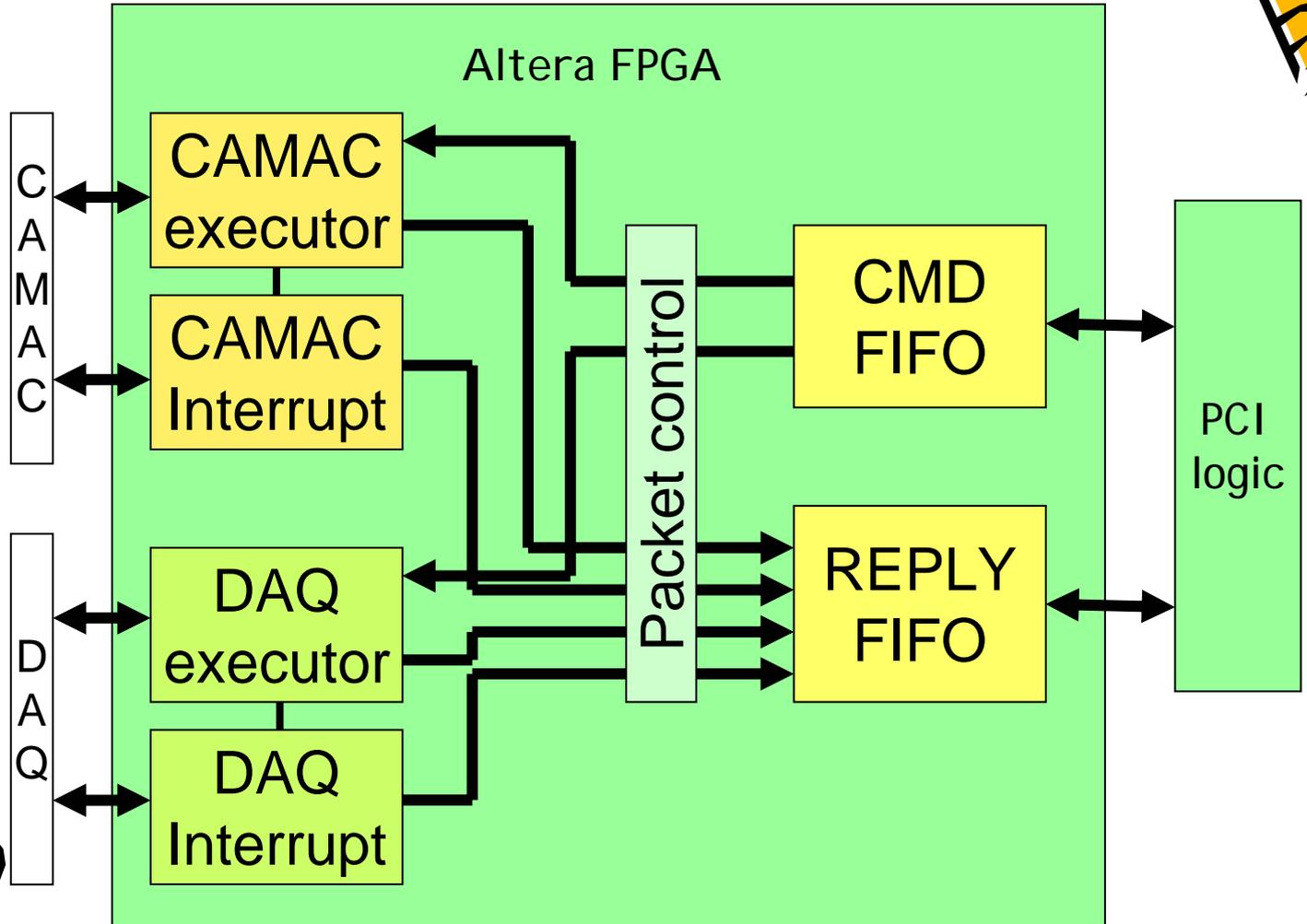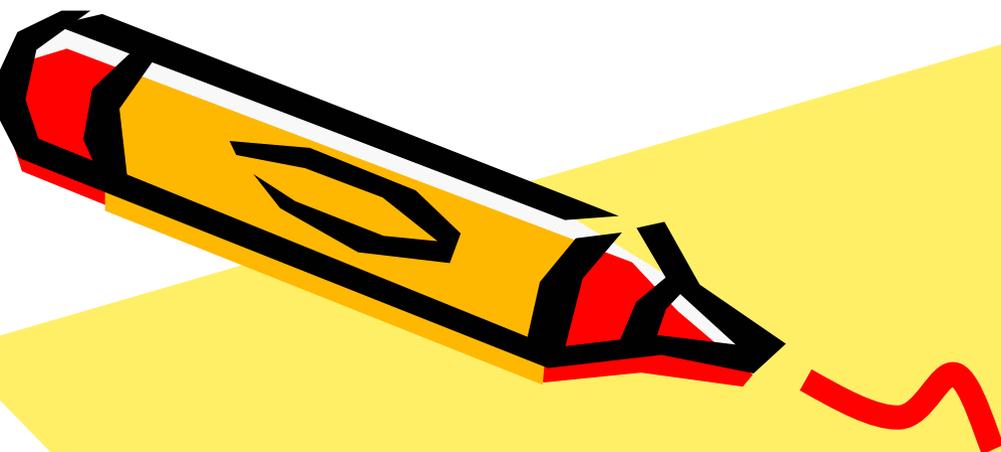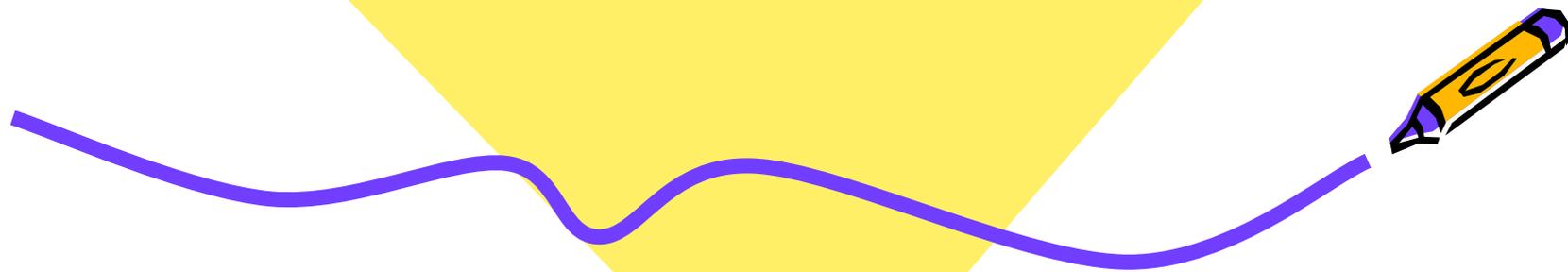
Frame format

64-bit fixed-length

Basic CAMAC operation

TX

cmd	N	A	F		24-bit DATA

RX

rply	N	A	F	ST	24-bit DATA
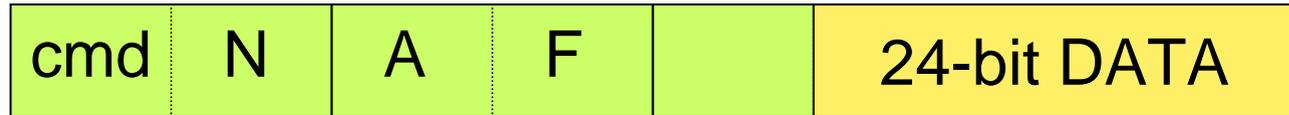
N:station, A:sub-address, F:function, ST:status(Q,X,...)
Read : data(tx) has no meaning.
Write : data(rx) has no meaning.
NDT : data(tx) and data(rx) have no meaning.

LAM(interrupt) CAMAC operation

RX

rply					24-bit LAM information
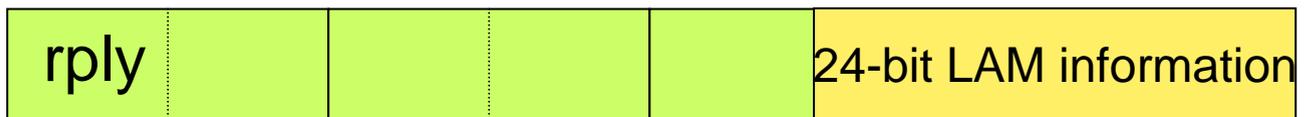
Frame format(cont.)

64-bit fixed-length

DAQ function(read event counter)

TX

cmd							

RX

rply			32-bit Event Counter
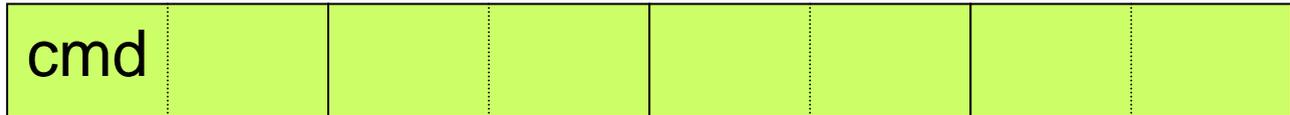
DAQ function(Trigger Interrupt)

RX

rply			32-bit Event Counter
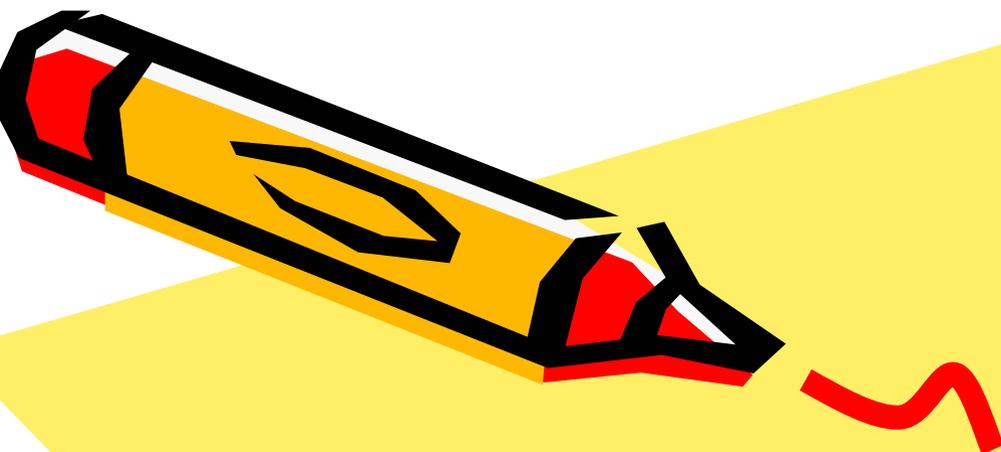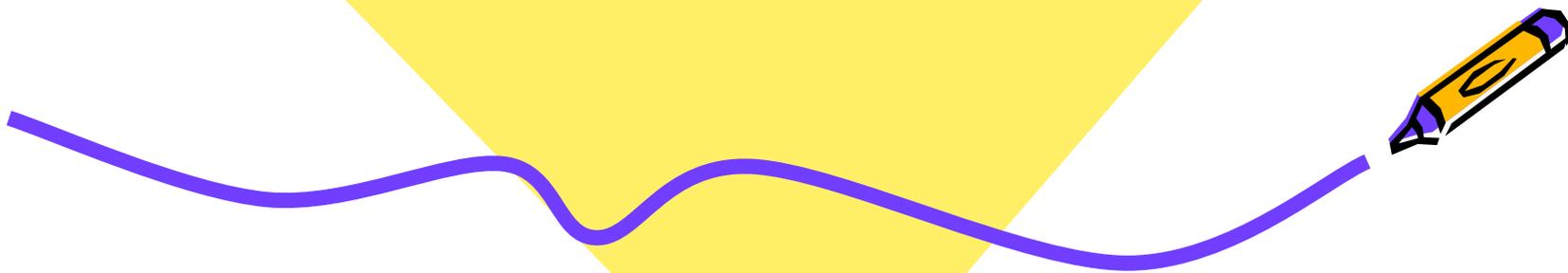
PCI operation

PCI operation

Programmed I/O :

       Generate CAMAC codes for CAMAC write/read/NDT;

       check whether TX FIFO is available;

       for(i=0;i<N;i++) {

              write data to TX data1/2 registers;

       }

       check whether RX FIFO is available;

       for(i=0;i<N;i++) {

              read data from RX data1/2 registers;

       }

       Extract CAMAC data and the status;

PCI operation (cont.)

Block transfer :

    Generate CAMAC code for CAMAC write/read/NDT;

    check whether TX FIFO is available;

    start reading data with non-blocking;

    write data with blocking.

    wait for the completion interrupt of the read operation;

    Extract CAMAC data and the status;

This algorithm makes CAMAC write and the read operate concurrently.
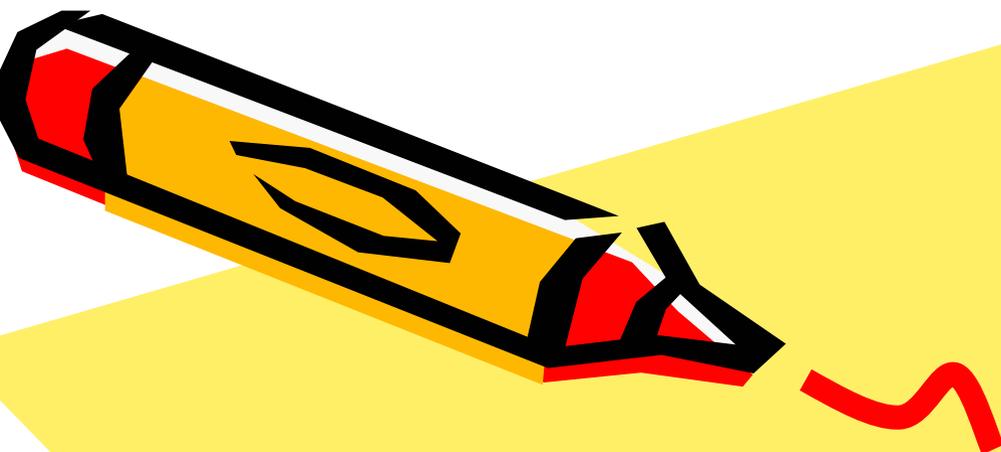
Performance Measurement
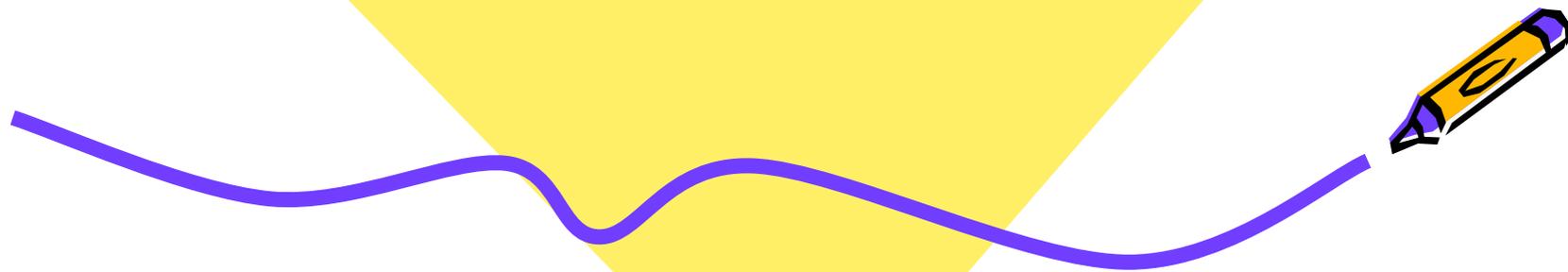
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CAMAC timing

Busy

S1

| Ch1 | 5.00 V | Ch2 | 5.00 V | M | 200ns | A | Ch1 ⌐ | 1.40 V |

CAMAC timing (cont.)

Busy

S1

Ch1 5.00 V   Ch2 5.00 V   M 1.00μs A Ch1 ⌐   1.40 V

T 10.00 %
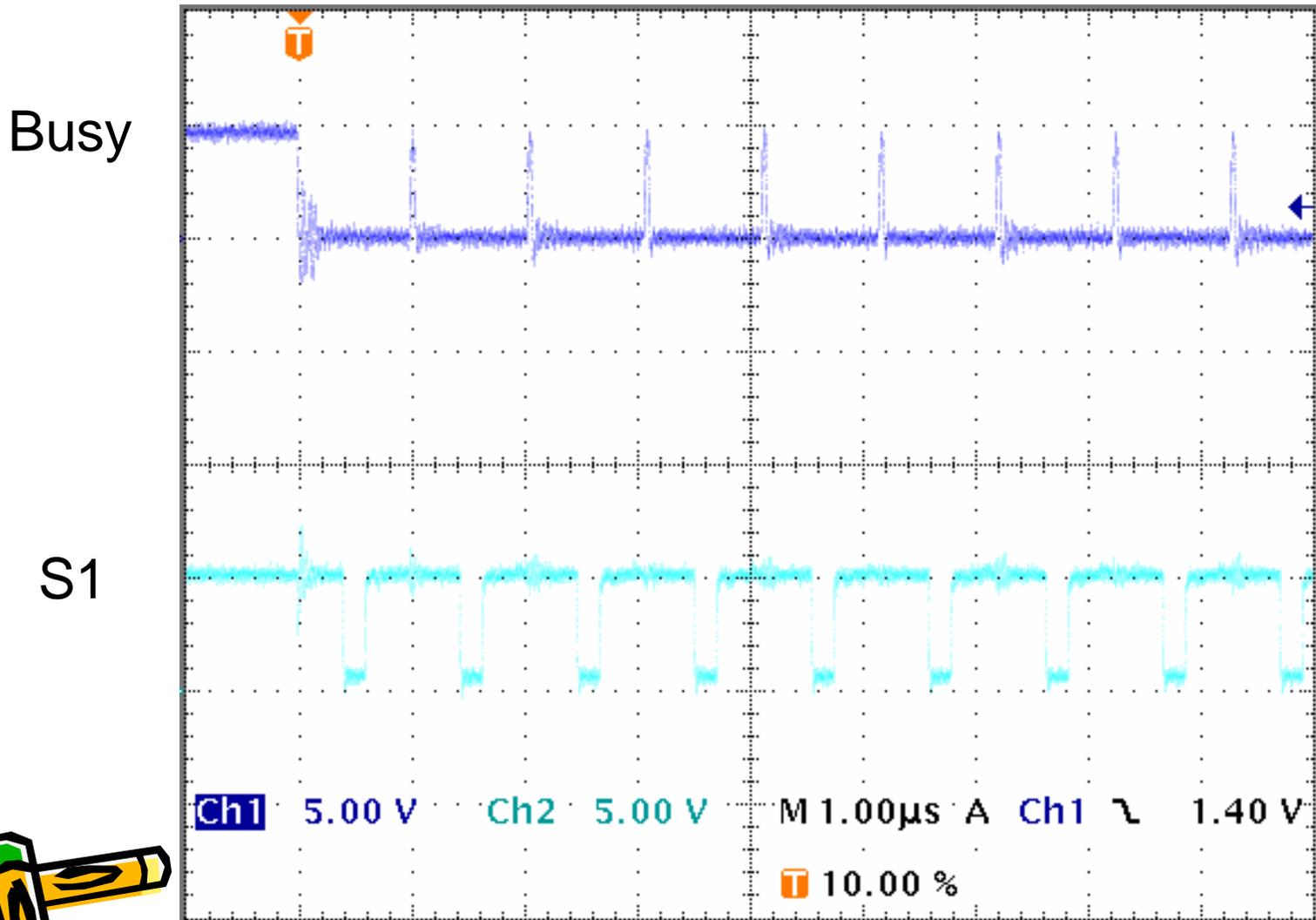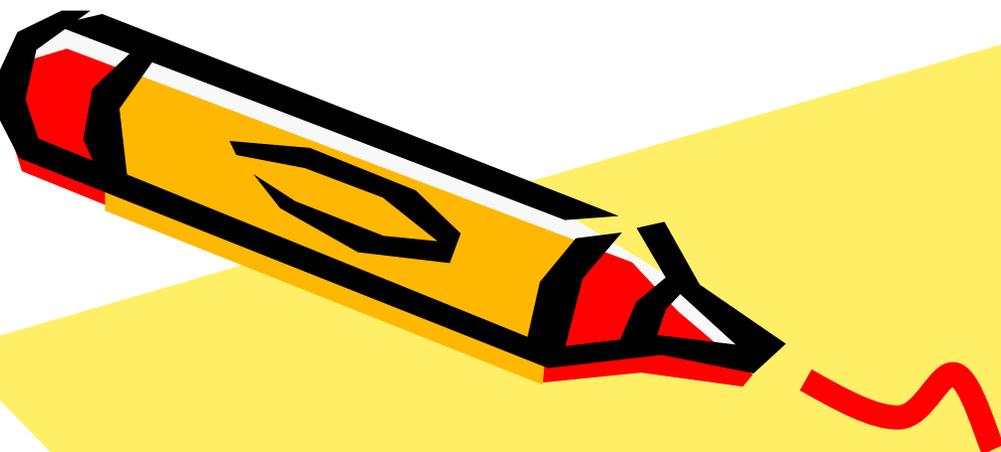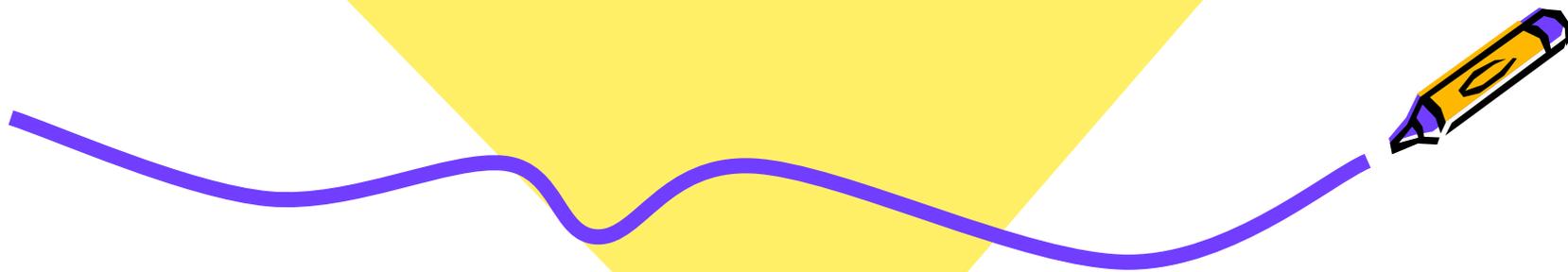
Current status and Plan

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Current status and Plan

- CAMAC/DAQ functions basically worked on the prototype of Pipeline CAMAC controller

- The prototype for mass production will be checked soon.

- USB interface for the CAMAC controller without board computer will be developed.

Related URLs

- http://www-online.kek.jp/~yasu/Parallel-CAMAC/
- http://www-online.kek.jp/~inoue/