KEK-VME crate backplane specification

2002/08/28 Ver 0

2003/06/28 Ver 1

1. Backplane Outline

1.1) Application: Custom VME backplane for high-energy physics experimentation. The backplane will be allocated to the 19” 9U sized subrack with 6U 160mm deep standard VME boards and 9U 400mm deep VME-physics boards.

1.2) Basic specification: VITA 1 and VME 64x: VITA 1.1

1.3) Backplane size and structure: 6U 21slot, according to Schroff design rule for the standard backplane.

2. Backplane detail specification

2.1) Connector and pin-out

See the Table 1.

Table 1

Slot	J1 connector Pin-out	J2 connector Pin-out	J0 connector Pin-out
1	IEC 61076-4-113, C160 (VME64x type) Pin-out is according to VITA1.1, VME64x. (VME bus passive termination)	IEC 61076-4-113, C160 (VME64x type) Pin-out is according to VITA1.1, VME64x. (VME bus passive termination)	IEC61076-4-101, HM, 19 pos. (VME64x J0 type), with short tail pins and without rear shroud Pin-out is specific defined. See the next clause.
2 - 21	DIN 41612, C96 (VME J1 type) with ADC Pin-out is according to VITA1.1. (VME bus passive termination)	DIN 41612, C96 (VME J2 type) Pin-out is according to VITA1.1. (VME bus passive termination)	IEC61076-4-101, HM, 19 pos. (VME64x J0 type), with short tail pins and without rear shroud Pin-out is specific defined. See the next clause

2.2) J0 connector pin-out definition

See the Table 2

Table 2

Pos.	z	a	b	c	d	e	f
1	GND	GND	GND	GND	GND	GND	GND
2	GND	GND	GND	GND	GND	GND	GND
3	GND	GND	GND	GND	GND	GND	GND
4	GND	+3.3V	+3.3V	+3.3V	+3.3V	+3.3V	GND
5	GND	+3.3V	+3.3V	+3.3V	+3.3V	+3.3V	GND
6	GND	+3.3V	+3.3V	+3.3V	+3.3V	+3.3V	GND
7	GND	+3.3V	+3.3V	GND	GND	GND	GND
8	GND	GND	GND	GND	GND	GND	GND
9	GND	GND	GND	GND	GND	GND	GND
10	GND	GND	GND	GND	-3.3V	-3.3V	GND
11	GND	-3.3V	-3.3V	-3.3V	-3.3V	-3.3V	GND
12	GND	-3.3V	-3.3V	-3.3V	-3.3V	-3.3V	GND
13	GND	GND	GND	GND	GND	GND	GND
14	GND	-5V	-5V	-5V	-5V	-5V	GND
15	GND	GND	GND	GND	GND	GND	GND
16	GND	S1+	S1-	GND	S2+	S2-	GND
17	GND	S3+	S3-	GND	S4+	S4-	GND
18	GND	S5+	S5-	GND	S6+	S6-	GND
19	GND	S7+	S7-	GND	S8+	S8-	GND

2.3) Specific signal bus line definition in the J0 connector

- 8 pair of the differential-signal bus line for the 100-Mbps LVDS (IT, SN65MLVD) are assigned as <S1+, S1->, <S2+, S2->, <S3+, S3->, <S4+, S4->, <S5+, S5->, <S6+, S6->, <S7+, S7-> and <S8+, S8-> in the J0.
- Characteristic line impedance of the differential-signal bus line: 100 Ohm

Backplane signal	Usage
S1	System clock distribution
S2	Trigger signal distribution
S3	Gate for analog digital processing
S4	Fast clear/reset during trigger acknowledge
S5	Event Tag 0(LSB)
S6	Event Tag 1
S7	Event Tag 2(MSB)

S8	Trigger acknowledge(BUSY)

- An example of the interface circuit of S1~8 are shown in Fig 1.
- Characteristic line impedance of the differential-signal bus line: 100 Ohm
- The data sheet of IT, SN65MLVD will be provided as the attached file.

2.1) Backplane power line current capacity for J0, -5V, +3.3V, and –3.3V

See the Table 3.

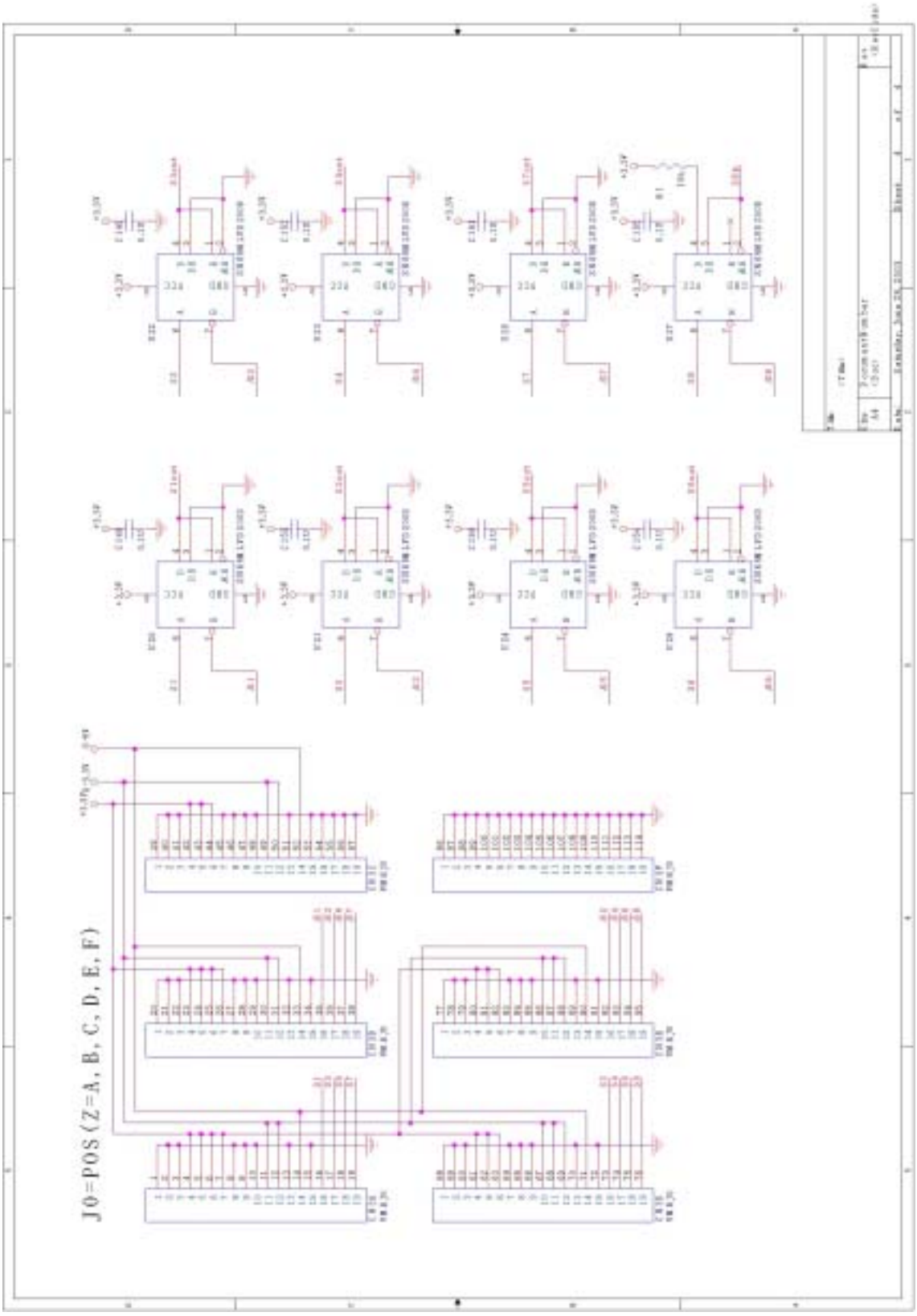
Table 3

Voltage	-5V	+3.3V	-3.3V
Total Max. Current	100A	320A	200A

Note:

1) Necessary power and GND layers have to be constructed in the backplane.

2) Necessary power-input terminals (power-bugs) have to be installed at rear side of the J1 and the J0 of the backplane.


J0=POS(Z=A, B, C, D, E, F)